IN THE CLAIMS

All currently pending claims are reproduced in their entirety.

1 (previously presented). A method of powering-up a memory cartridge in a computer system, comprising the acts of:

(a) inserting the memory cartridge into the computer system while the computer system is operating;

(b) initializing the memory cartridge while the computer system is operating;

(c) rebuilding the memory cartridge while the computer system is operating; and

(d) verifying the memory cartridge for validity while the computer system is operating.

2 (cancelled).

3 (previously presented). The method, as set forth in claim 1, wherein act (a) comprises the acts of:

sequentially connecting a plurality of pins at an interface, the interface comprising a connector configured to couple the memory cartridge to the computer system in response memory cartridge being inserted into the computer system; and

sequentially enabling a plurality of signals in response to the sequential connection of the plurality of pins.

4 (original). The method, as set forth in claim 3, wherein the plurality of pins comprise varying pin lengths, the pin lengths assigned to sequentially connect the plurality of pins upon insertion memory cartridge into the computer system.

5 (previously presented). The method, as set forth in claim 1, wherein act (a) comprises:

connecting one or more ground pins from the memory cartridge to the computer system;

connecting one or more power pins from the memory cartridge to the computer system;

connecting one or more first insertion removal sense pins from the memory cartridge to the computer system;

connecting one or more data pins from the memory cartridge to the computer system; and

connecting one or more second insertion removal sense pins from the memory cartridge to the computer system.

6 (original). The method, as set forth in claim 5, wherein the act of connecting the one or more first insertion removal sense pins causes the assertion of a power signal to a power controller.

7 (original). The method, as set forth in claim 6, wherein the assertion of the power signal to the power controller activates power transistors to provide power to the memory cartridge.

8 (original). The method, as set forth in claim 7, wherein the power controller monitors the voltage level at an output of the power transistors and connects a system clock to the memory cartridge when the voltage level reaches a minimum threshold.

9 (original). The method, as set forth in claim 5, wherein the act of connecting the one or more second insertion removal sense pins generates an interrupt from a host controller indicating that the memory cartridge has been installed.

10 (previously presented). The method, as set forth in claim 1, wherein act (a) comprises the act of locking the memory cartridge into the memory system.

11 – 15 (cancelled).

16 (previously presented). A computer system comprising:

a host controller; and

a memory sub-system coupled to the host controller and configured to operate in a redundant mode of operation and a non-redundant mode of operation, the memory sub-system comprising:

a memory system board, the memory system board comprising an indicator configured to notify of user of errors in the memory sub-system;

a plurality of memory cartridges coupled to the system board and configured to store data;

a plurality of cartridge connectors coupled to the memory system board, each of the plurality of memory cartridges connectors configured to receive one of the plurality of memory cartridges and further configured to facilitate the insertion and removal of the memory cartridges while the system is powered-up; and

a plurality of control logic devices coupled to the memory system board and configured to facilitate the transition of the memory sub-system from the redundant mode of operation to the non-redundant mode of operation, and further configured to facilitate the transition of the memory sub-system from the non-redundant mode of operation to the redundant mode of operation.

17 (original). The computer system, as set forth in claim 16, wherein the host controller comprises error detection logic configured to detect errors in the data stored in the memory cartridges.

18 (original). The computer system, as set forth in claim 16, wherein the host controller comprises a plurality of drivers configured to drive the plurality of control logic devices.

19 (original). The computer system, as set forth in claim 16, wherein the indicator comprises a plurality of light devices, each of the plurality of light devices coupled to a light emitting diode and configured to illuminate in response to error detection;

20 (original). The computer system, as set forth in claim 16, wherein each of the plurality of memory cartridges comprises a plurality of memory modules.

21 (original). The computer system, as set forth in claim 20, wherein each of the plurality of memory cartridges comprises four memory modules.

22 (original). The computer system, as set forth in claim 20, wherein each of the plurality of memory modules comprises a Dual Inline Memory Module (DIMM).

23 (original). The computer system, as set forth in claim 20, wherein each of the plurality of memory modules comprises a plurality of memory devices configured to store data.

24 (original). The computer system, as set forth in claim 23, wherein each of the plurality of memory devices comprises a Synchronous Dynamic Random Access Memory (SDRAM) device.

25 (original). The computer system, as set forth in claim 16, wherein the memory sub-system comprises five memory cartridges.

26 (original). The computer system, as set forth in claim 16, wherein each of the plurality of memory cartridges comprises a memory control device configured to control access to one of the plurality of memory cartridges.

27 (original). The computer system, as set forth in claim 26, wherein each of the memory control devices comprises error detection logic configured to detect errors in the data stored in the plurality of memory cartridges.

28 (original). The computer system, as set forth in claim 16, wherein each of the plurality of cartridge connectors comprises a plurality of pins of varying lengths.

29 (original). The computer system, as set forth in claim 19, wherein each of the plurality of light devices is associate with one of a memory cartridge and a DIMM.

30 (original). The computer system, as set forth in claim 26, wherein each of the plurality of control logic devices comprises:

a first device programmed to facilitate the exchange of a first set of control signals between the host controller and the memory sub-system;

a plurality of power control devices coupled to the first device and configured to provide power fault detection in the computer system; and

a plurality of second devices coupled between the memory control device and the host controller and programmed to exchange a second set of control signals there between.

31 (original). The computer system, as set forth in claim 30, comprising a plurality of devices configured to provide an audio alarm for the memory sub-system, the alarm being activated in the event of an illegal memory cartridge removal.

32 (original). The computer system, as set forth in claim 30, wherein the first device is a programmable array logic (PAL) device.

33 (original). The computer system, as set forth in claim 30, wherein the first set of control signals comprise Present Detect signals, Power Fault signals, and Pre-Insertion Removal Notification Cable signals.

34 (original). The computer system, as set forth in claim 30, wherein each of the plurality of power control devices is configured to facilitate a soft start of the memory cartridge.

35 (original). The computer system, as set forth in claim 30, wherein each of the plurality of power control devices is configured to provide over-current protection for the memory cartridge.

36 (original). The computer system, as set forth in claim 30, wherein each of the plurality of power control devices is configured to provide under-voltage protection for the memory cartridge.

37 (original). The computer system, as set forth in claim 30, wherein each of the plurality of second devices comprises a programmable array logic (PAL) device.

38 (previously presented). The computer system, as set forth in claim 30, wherein the second set of control signals comprises a plurality of interrupt signals and a plurality of control signals.